DESCRIPTION

TRENCH-GATE SEMICONDUCTOR DEVICES AND THEIR MANUFACTURE

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THIS IS A CONTINUATION OF ~~10/213,460~~ US PAT 6,800,900

This invention relates to trench-gate semiconductor devices, for example power MOSFETs (insulated-gate field-effect transistors), and their manufacture.

Published Japanese patent application Kokai JP-A-2001-24193 and its English-language abstract in Patent Abstracts of Japan describe cellular trench-gate semiconductor devices comprising active device cells in a cellular area of a semiconductor body, and a device termination structure that extends around the whole perimeter of the cellular area. The whole contents of Kokai JP-A-2001-24193 and its said English-language abstract are hereby incorporated herein as reference material.

Each active device cell has a channel-accommodating region of a second conductivity type between a surface-adjacent source region and an underlying drain region that are of a first conductivity type. An insulated gate trench accommodating the trench-gate extends from the source region through the channel-accommodating region and into the underlying drain region. The trench-gate is dielectrically coupled to the channel-accommodating region by an intermediate gate dielectric layer at sidewalls of the gate trench.

The particular device termination structures disclosed in JP-A-2001-24193 include:

- an end region 4(p) of the second conductivity type having a higher doping concentration than the channel-accommodating region 8(p),
- an end trench 5B that is an extension of the insulated gate trench 5A into the end region 4(p) and that accommodates an extension 7B of the trench-gate 7A,
- and a conductive layer 7C that is connected to the extension of the trench-gate and extends over an intermediate insulating layer 3,6 over the end region 4(p).

processing at different stages. By this means, narrow trench-gates can be formed (narrower than the window), and the source region and a contact window for a source electrode can be determined in a self-aligned manner with respect to this narrow trench. The whole contents of US-A-6,087,224 are hereby incorporated herein as reference material.

BRIEF DESCRIPTION OF DRAWINGS

Various advantageous features in accordance with the present invention are set out in the appended claims. These and others are illustrated in embodiments of the invention that are now described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a simple plan view of one example of a trench-gate semiconductor device in accordance with the invention, showing both edge-termination and bus-bar configurations at the gate-connection level on top of trench-etch mask areas;

Figure 2 is a cross-sectional view of one example of edge termination for such a device as that of Figure 1, taken on the line II-II of Figure 1;

Figure 3 is a cross-sectional view of a corresponding example of an inside part of such a device as that of Figure 1, taken on the line III-III of Figure 1, i.e. through a gate bus-bar structure;

Figures 4 and 5 are enlarged cross-sectional views of parts of an active-cell area and an end-structure area respectively of Figures 1 to 3;

Figures 6 to 11 are cross-sectional views of the device part of Figure 5 at successive stages in its manufacture by one example of a method in accordance with the present invention;

Figures 12 and 13 are cross-sectional views of a device part similar to that of Figure 5, but showing modifications that are also in accordance with the present invention;

Figures 14 and 15 are cross-sectional views of two different device terminations (i.e. some similarity to that of Figure 2), showing modifications that are also in accordance with the present invention; and